Low Noise Amplifier for 3.5 GHz using the Avago ATF-35143 Low Noise PHEMT

Application Note 1271

Introduction

This application note describes a low noise amplifier for use in the 3.4 GHz to 3.8 GHz wireless local loop, wireless broadband access, and digital microwave radio markets. The circuits are designed for use with 0.031 inch thickness FR-4 printed circuit board material. The amplifiers make use of low cost, miniature, multilayer chip inductors for small size. When biased at a V_{ds} of 3 volts and I_{ds} of 30 mA, the Avago ATF-35143 amplifier will provide 12.5 to 13.5 dB gain , 0.9 dB noise figure and an output intercept point (IP3) of +27 to +29 dBm. An active bias solution using dual power supply techniques is discussed. The design goals are summarized in Table 1.

The design is based on 0.813 mm (0.031 inch) thickness Grade FR4 copper laminate epoxy glass PC material. The amplifier schematic is shown in Figure 1, with component values in Table 2.

Description

The Avago Technologies ATF-35143 is one of a family of high dynamic range low noise PHEMT devices designed for use in low cost commercial applications in the VHF through 6 GHz frequency range. The ATF-35143 is a 400 micron gate width device with 2 GHz performance tested and guaranteed at a V_{ce} of 2 V and I_d of 15 mA. The ATF-35143 is housed in a 4-lead SC-70 (SOT-343) surface mount plastic package.

LNA Design

The amplifier was designed for a V_{ds} of 3 volts and an I_{ds} of 30 mA. The amplifier schematic is shown in Figure 1. Typical power supply voltage, V_{dd}, would be in the 5 volt range. The generic demo board shown in Figure 2 is used. The board gives the designer several

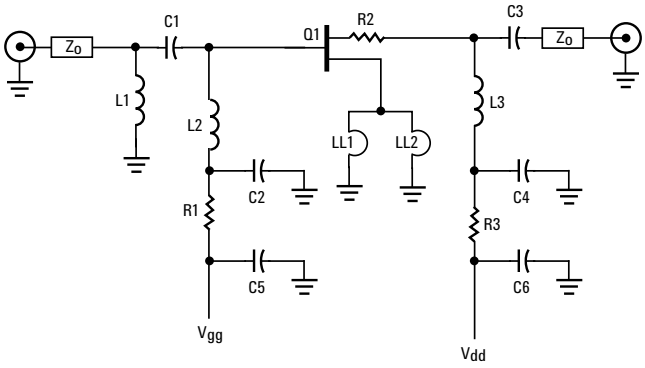

Figure 1. The Amplifier Schematic

Table 1. Design Goals

Parameter at 3.5 GHz	Value
Gain	13.4 dB
Noise Figure, dB	0.9 dB
Output 3rd Order Intercept Point	27 dBm
Input 3rd Order Intercept Point	13.6 dBm
Output P-1dB Compression	14.5 dBm
Input return loss	24 dB
Output return loss	12.3 dB
Supply Current	30 mA
BW	3.4 - 3.8 GHz

design options for both the rf circuitry and biasing options. The demo board was designed such that the input and output impedance matching networks can be either lumped element networks or etched microstrip networks for lower cost. Either low pass or high pass structures can be generated based on system requirements. The demo board also allows the FET to be either self biased or with grounded sources the FET can be biased with a negative voltage applied to the gate terminal. The demo board is etched on 0.031" thickness FR-4 material for cost considerations.

Biasing Options and Source Grounding

Passive biasing schemes are generally preferred for their simplicity. One method of passive biasing requires the source leads be direct dc grounded. A negative voltage is applied to the gate through a bias de-coupling network. The gate voltage is then adjusted for the desired value of drain current. The gate voltage required to support a desired drain current, I_d, is dependent on the device's pinchoff voltage, V_p, and the saturated drain current, I_{dss}. I_d is calculated with the following equation.

$$V_{gs} = V_p \left(1 - \sqrt{\frac{I_d}{I_{dss}}}\right)$$

Values for V_{gs} may be calculated from the typical I-V curves found in the data sheet.

The use of a controlled amount of source inductance can often be used to enhance LNA performance. Usually only a few tenths of a nanohenry or at most a few nanohenrys of inductance is required. This is effectively equivalent to increasing the source leads by only 0.050 inch or so. The effect can be easily modeled using Avago Technologies ADS®. The usual side effect of excessive source inductance is very high frequency gain peaking and resultant oscillations. The larger gate width devices have less high frequency gain and therefore the high frequency performance is not as sensitive to source inductance as a smaller device would be. The ability of the 400 micron gate width ATF-35143 to tolerate greater source inductance allows the designer to take advantage of self biasing thereby only necessitating a single positive power supply.

Design of ATF-35143 Amplifier

The parts list for the first amplifier is shown in Table 2. The demo board as modified is shown in Figure 3. The modifications are discussed in the next section.

The amplifier uses a high-pass impedance matching network for the noise match. The high-pass network consists of a series capacitor (C1) and a shunt inductor (L1). The demo board incorporates series microstripline on the input. It is not required for this amplifier design and can be removed from the demo board. It should be replaced with a shunt inductor, L3. The circuit loss will directly relate to noise figure, thus Q of L3 is extremely important. The Toko LL1005-FH3N3 or similar device is suitable for this purpose. Shunt inductor (L1) provides low frequency gain reduction, which can minimize the amplifier's susceptibility to low frequency transmitter overload. It is also part of the input matching network along with C1. C1 also doubles as a dc block. L2 also doubles as a means of inserting gate voltage for biasing up the PHEMT. This requires a good bypass capacitor in the form of C2. The Q of L2 is also extremely important from the standpoint of circuit loss, which will directly relate to noise figure. The Toko LL1005-FH2N2S is a small multilayer chip inductor with a rated Q of 30 at 800 MHz. Lower element

Table 2. Component Parts List for the ATF-35143 Amplifier.

C1	1.5 pF chip capacitor (C1005COG1H1R5C)
C2, C4	4.0 pF chip capacitor (C1005COG1H040C)
C3	2.0 pF chip capacitor (C1005COG1H020C)
C5, C6	1000 pF chip capacitor
L1	2.2 nH inductor (Toko LL1005-FH2N2S)
L2, L3	3.3 nH inductor (Toko LL1005-FH3N3)
LL1, LL2	Strap each source pad to the ground pad with 0.030" wide etch. The jumpered etch is placed a distance of 0.037" away from the point where each source lead contacts the source pad.
Q1	Avago Technologies ATF-35143 PHEMT
R1	47 Ω chip resistor
R2	10 Ω chip resistor (Murata CR05-10RJ)
R3	53 Ω chip resistor
Zo	50 Ω Microstripline

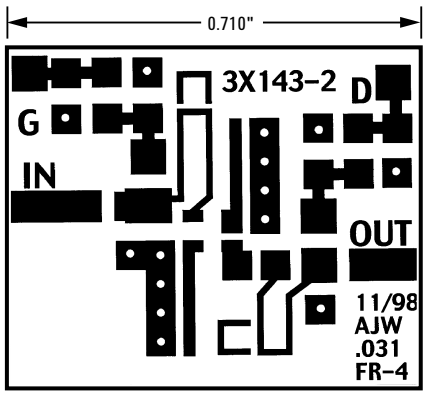

Figure 2. Artwork for the ATF-35143 Low Noise Amplifier.

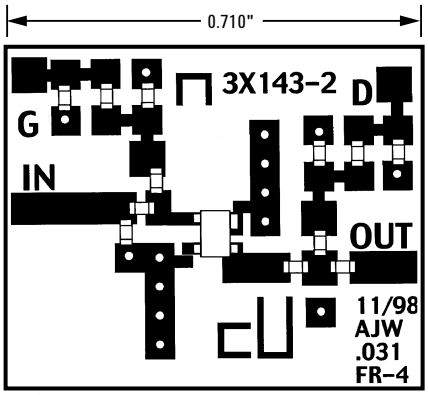

Figure 3. Component Placement Drawing for the ATF-35143 Low Noise Amplifier

Qs may increase circuit noise figure and should be considered carefully. This network has been a compromise between low noise figure, input return loss and gain. Resistor R2 and capacitors C2 and C4 provide in-band stability while resistors R1 and R3 provide low frequency stability by providing a resistive termination.

Inductors LL1 and LL2 are actually very short transmission lines between each source lead and ground. The inductors act as series feedback. The amount of series feedback has a dramatic effect on in-band and out-of-band gain, stability and input and output return loss. The amplifier demo board is designed such that the amount of source inductance is variable. Each source lead is connected to a microstrip line, which can be connected to a ground pad at any point along the line. For minimal inductance, the source lead pad is connected to the ground pad with a very short piece of etch at the point closest to the device source lead. For the amplifier, each source lead is connected to its corresponding ground pad at a distance of approximately 0.037" from the source lead. The 0.037" is measured from the edge of the source lead to the closest edge of the first via hole. The remaining unused source lead pad should be removed by cutting off the unused etch. On occasion, the unused etch which looks like an open circuited stub has caused high frequency oscillations. During the initial prototype stage, the amount of source inductance can be tuned to optimize performance. More on this subject next.

Determining the Optimum Amount of Source Inductance

Adding additional source inductance has the positive effect of improving input return loss and low frequency stability. A potential down side is reduced low frequency gain, however, decreased gain also correlates to higher input intercept point. The question then becomes how much source inductance can one add before one has gone too far?
For an amplifier operating in the 900 MHz frequency range, excessive source inductance will manifest itself in the form of a gain peak in the 6 to 10 GHz frequency range. Normally the high frequency gain roll-off will be gradual and smooth. Adding source inductance begins to add bumps to the once smooth roll-off. The source inductance, while having a degenerative effect at low frequencies, is having a regenerative effect at higher frequencies. This shows up as a gain peak in S21 and also shows up as input return loss S11 becoming more positive. Some shift in upper frequency performance is acceptable as long as the amount of source inductance is fixed and has some margin in the design so as to account for S21 variations in the device.

Performance of the Avago ATF-35143 Amplifier

The amplifier is biased at a V_{ds} of 3 volts and I_d of 30 mA. Typical V_{gs} is -0.41 volts. The measured noise figure and gain of the completed amplifier is shown in Figures 4 and 5. Noise figure is a nominal 1.0 dB from 3.0 through 4.0 GHz. Gain is a minimum of 11.5 dB at 4.0 GHz with a peak of 15.0 dB at 2.8 GHz.

Measured input and output return loss is shown in Figure 6. The input return loss at 3.5 GHz is 24 dB with a corresponding output return loss of 12.3 dB. Note that best input return loss and minimum noise figure do not necessarily occur at the same frequency. This is due to Γo and S11* not occurring simultaneously at any one frequency. The amplifier output intercept point (OIP3) was measured at a nominal +27 dBm at a dc bias point of 3 volts V_{ds} and an I_d of 30 mA. P-1dB measured +14.5 dBm.

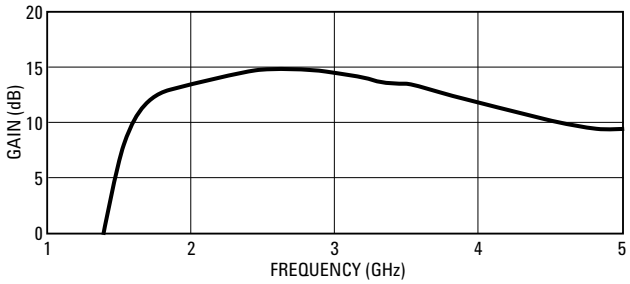

Figure 4. Gain vs. Frequency

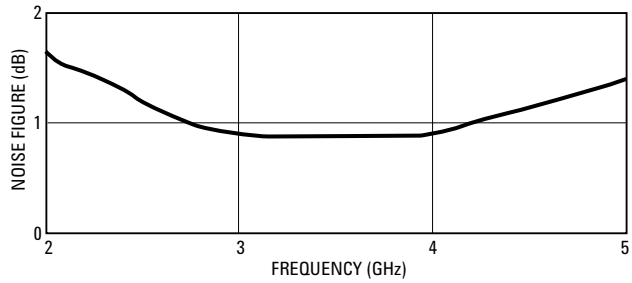

Figure 5. Noise Figure vs. Frequency

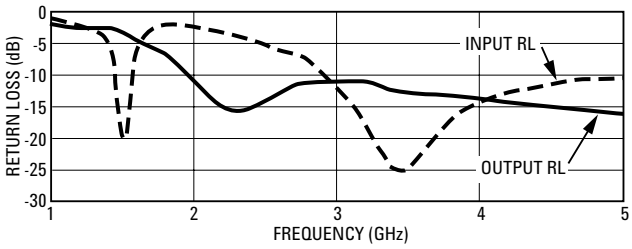

Figure 6. Input and Output Return Loss vs. Frequency

Avago ATF-35143 Low Noise Amplifier Design

Using Avago Technologies Eesof Advanced Design System Software the amplifier circuit can be simulated in both linear and nonlinear modes of operation. The original design draft was a low noise amplifier with an Output Third Order Intercept Point (OIP3) of 26-28 dBm with a noise figure close to 1.0 dB at 3.5 GHz.

Linear Analysis

The circuit used for the linear analysis is shown in Figure 7. The ATF35143.s2p file can be downloaded from the Avago Wireless Design Center web site. The 2-Port S-parameter file icon available from the linear Data File Palette is used. A template for s-parameter evaluation is available in ADS, the Sparams_wNoise template was chosen. The circuit components were added to the simulation circuit. The more detailed the simulation the more accurate the results will be. An accurate circuit simulation can provide the appropriate first step to a successful amplifier design. The inductance associated with the chip capacitors and resistors was included in the simulation. Where possible models were chosen from the ADS SMT component library. Models of SMT components can also be obtained from the manufacturers' web sites. Manufacturing tolerances in both the active and passive components often prohibit perfect correlation. The results of the simulated noise figure, gain, input and output return losses are shown in Figures 8, 9 and 10. The linear simulated performance of the amplifier was very close to the measured results.

As noted on the data sheet, the ATF-35143 S and Noise Parameters are tested in a fixture that includes plated through holes through a 0.025" thickness printed circuit board. Due to the complexity of de-embedding these grounds, the S and Noise Parameters include the effects of the test fixture grounds. Therefore, when simulating a 0.031" thickness printed circuit board, only the difference in the printed circuit board thickness is included in the simulation, i.e. 0.031" - 0.025" = 0.006". The transmission lines that connect each source lead to its corresponding plated through hole is simulated as a microstripline (MLIN).

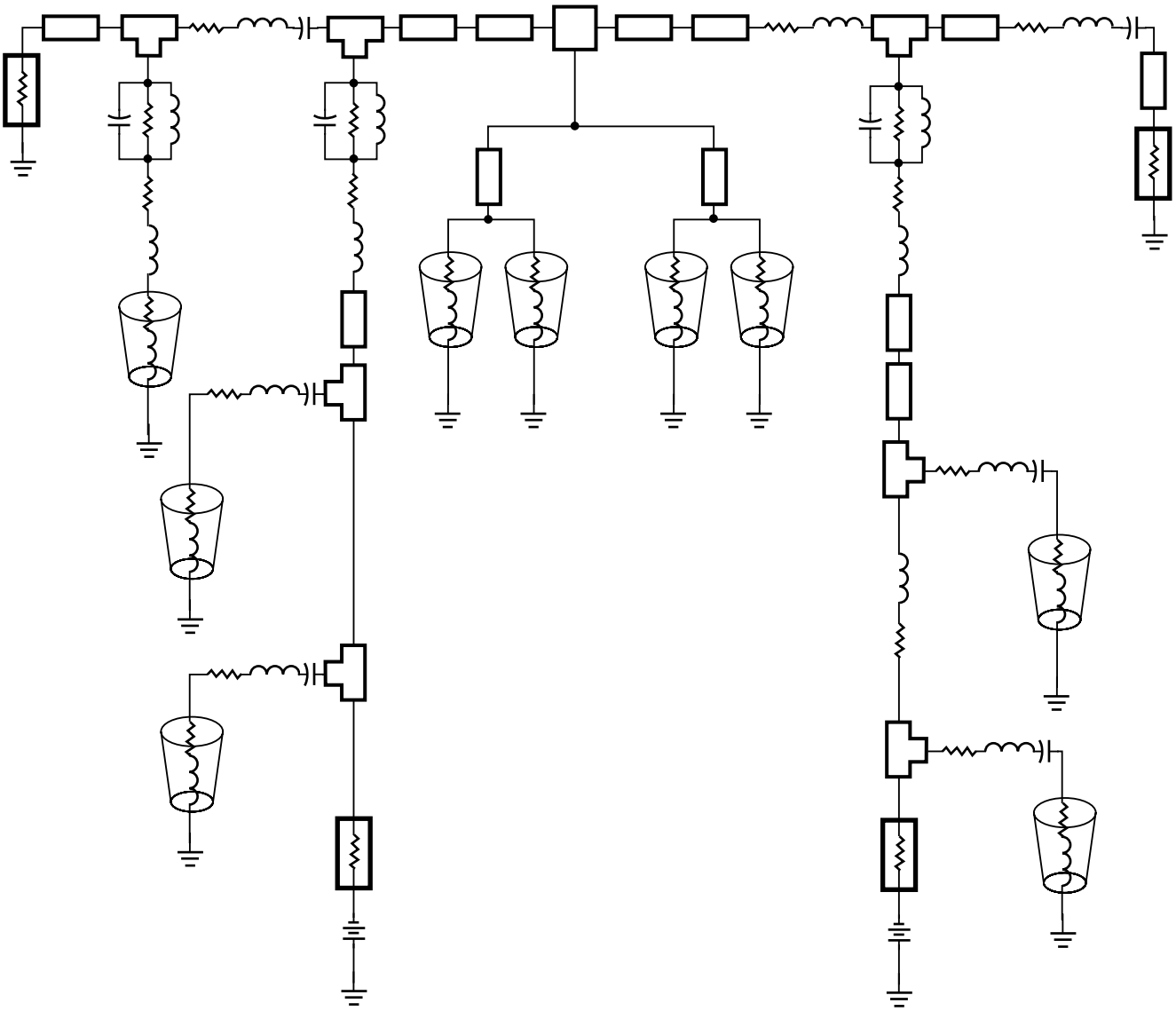

Figure 7. ADS Schematic

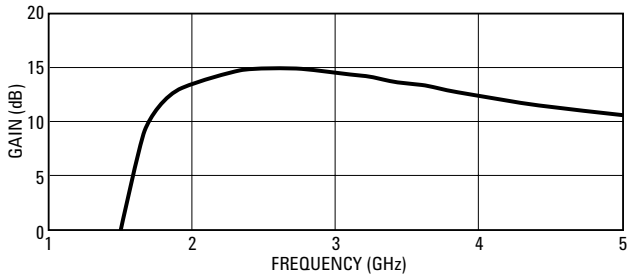

Figure 8. Linear Simulated Gain vs. Frequency

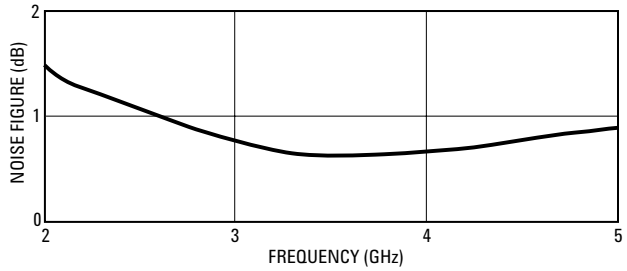

Figure 9. Linear Simulated Noise Figure vs. Frequency

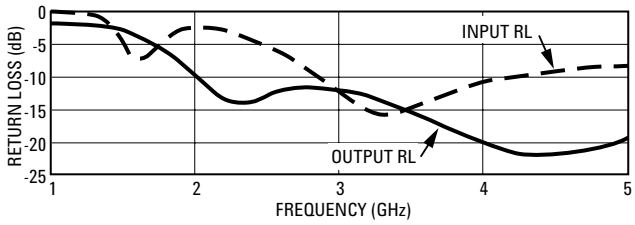

Figure 10. Linear Simulated Input and Output Return Loss vs. Frequency

Non-Linear Analysis

The circuit that is used for the non-linear analysis is identical to the linear analysis circuit. The 2-Port S-parameter file icon was replaced by the non-linear model for the ATF-35143. The model was downloaded from the Avago Wireless Design Center. The ADS unarchive function was used to extract the model. See ADS for further details on unarchiving models.

To perform the non-linear analysis the Harmonic Balanced controller or one of the other non-linear simulators, must be inserted into the schematic window. The current probe and the node point were inserted to check that the bias conditions were correct.

The results of the simulated noise figure, gain, input and output return losses are shown in Figures 11, 12 and 13. The Non-Linear simulator allows Avago to simulate the P-1dB and the Output Third Order Intercept Point. The amplifier OIP3 was simulated at +27.9 dBm and P-1dB +14.8 dBm. Non-linear simulated performance of the amplifier was very close to the measured results. A summary of the Non-linear simulated performance is shown in Table 3.

Table 3. Summary of Non-linear Simulated Performance

Bias Conditions	Noise Figure	P-1dB	Third Order Intercept
2 V, 15 mA	0.7 dB	9.8 dBm	22.1 dBm
2 V, 30 mA	0.6 dB	12.9 dBm	27.5 dBm
3 V, 30 mA	0.6 dB	14.8 dBm	27.9 dBm

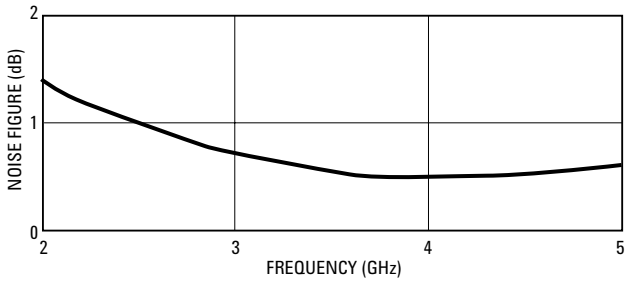

Figure 11. Non-Linear Simulated Noise Figure vs. Frequency

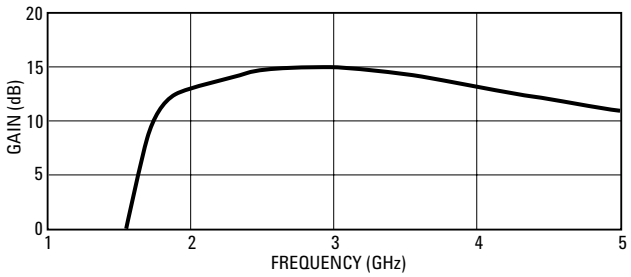

Figure 12. Non-Linear Simulated Gain vs. Frequency

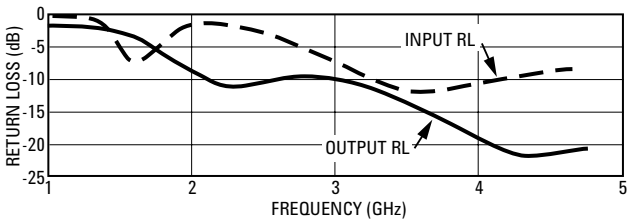

Figure 13. Non-Linear Simulated Input and Output Return Loss

Circuit Stability

Besides providing important information regarding gain, noise figure, input and output return loss, the computer simulation provides very important information regarding circuit stability. Unless a circuit is actually oscillating on the bench, it may be difficult to predict instabilities without actually presenting various VSWR loads at various phase angles to the amplifier. Calculating the Rollett Stability factor K and generating stability circles are two methods made considerably easier with computer simulations.

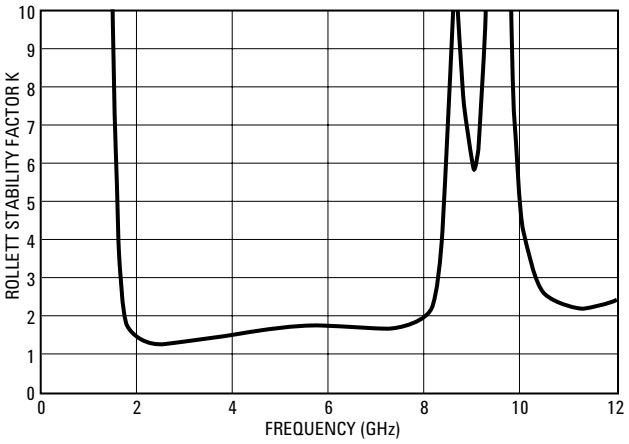

Figure 14. Simulated Rollett Stability Factor K

The simulated gain, noise figure, and input/output return loss of the ATF-35143 amplifier are shown in Figures 8, 9 and 10. These plots only address the performance near the actual desired operating frequency. It is still important to analyze out-of-band performance in regards to abnormal gain peaks, positive return loss and stability. A plot of Rollett Stability factor K as calculated from 0.1 GHz to 12 GHz is shown in Figure 14 for the amplifier. Emitter inductance can be used to help stability. It should be noted however that excessive inductance will cause high frequency stability to get worse (i.e., decreased value of K). The resistive loading, R2, is one of the main contributors to stability along with the inductance in the ground path. Increasing the value of R2 will make the stability factor K higher. As stability is improved, certain amplifier parameters such as gain and power output may have to be sacrificed.

Conclusion

The amplifier design has been presented using the Avago Technologies ATF-35143 low noise PHEMT. The ATF-35143 provides a very low noise figure along with high intercept point making it ideal for applications where high dynamic range is required. In addition to providing low noise figure, the ATF-35143 can be simultaneously matched for very good input and output return loss, making it easily cascadable with other amplifiers and filters with minimal effect on system passband gain ripple.

References

Performance data for the Avago ATF-35143 PHEMT may be found on http://www.Avago.com/view/rf

Application Notes

Application Note 1197, “A Low Current, High Intercept Point, Low Noise Amplifier for 1900 MHz using the Avago ATF-38143 Low Noise PHEMT”

Application Note 1174, “Low Noise Amplifiers for 1600 MHz and 1900 MHz Low Current Self-biased Applications using the ATF-35143 Low Noise PHEMT”

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