DISSIPATION LIMITER

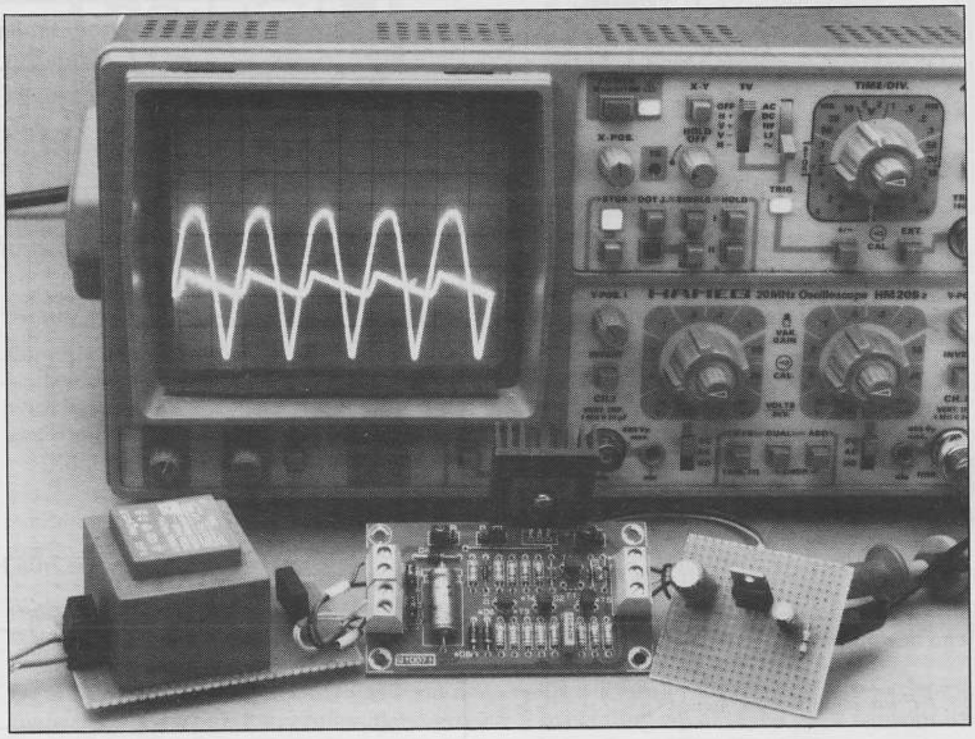
by C. Zschocke

Dissipation in electronically regulated power supplies, manifested by heat, is a problem that is normally tackled by providing external heat sinks. The limiter presented here offers a more intelligent solution. It can be used as an add-on unit with virtually any power supply.

THE secondary alternating voltage in power supplies stabilized with the aid of series regulators is normally calculated to ensure that with maximum output voltage and current the potential across the reservoir capacitor does not drop below the minimum voltage, U_r, required for satisfactory operation of the regulator. When the supply operates below maximum output voltage and current, the power that is then not required is converted into heat. Moreover, the design allows for maximum output voltage and current even when the mains voltage is at its lowest specified level.

The secondary voltage may well be specified too high, with the result that when the mains voltage is at its highest specified level and the power supply is open-circuited, the maximum permissible potential across the reservoir capacitor, and thus that at the input of the regulator, may easily be exceeded.

It is clear that in most power supplies, the specified voltage levels for the regulator and reservoir capacitor are needlessly high.



Possible solutions

The uneconomical design outlined above may be improved in several ways. It is, for instance, possible, with the aid of relays, to select secondary alternating voltages according to the load requirement. This is, however, possible only with a very special, and therefore expensive, mains transformer. Another possibility is to use phase gating control. This, however, requires fairly high switching currents and causes noise on the mains supply. Moreover, capacitors that can withstand high current pulses must be used and these are expensive.

A third method is used in the circuit presented here. In this, the charging of the reservoir capacitor is interrupted when a certain potential across the capacitor is reached. The circuit, which can be added to most existing regulated mains power supplies,

- minimizes the power dissipation;
- offers an additional reduction in dissipation during a short-circuit or during current limiting;
- is inexpensive to build;
- uses only standard, readily available components;
- needs only little space;
- is suitable for high-current supplies;
- can be used with positive and negative series regulators.

Principle of operation

In Figure 1, an electronic switch, for instance, a SIPMOS transistor, is inserted between the rectifier and the reservoir capacitor. At the start of each half cycle, the switch is on (U_r>3 V). A charging current flows into the capacitor

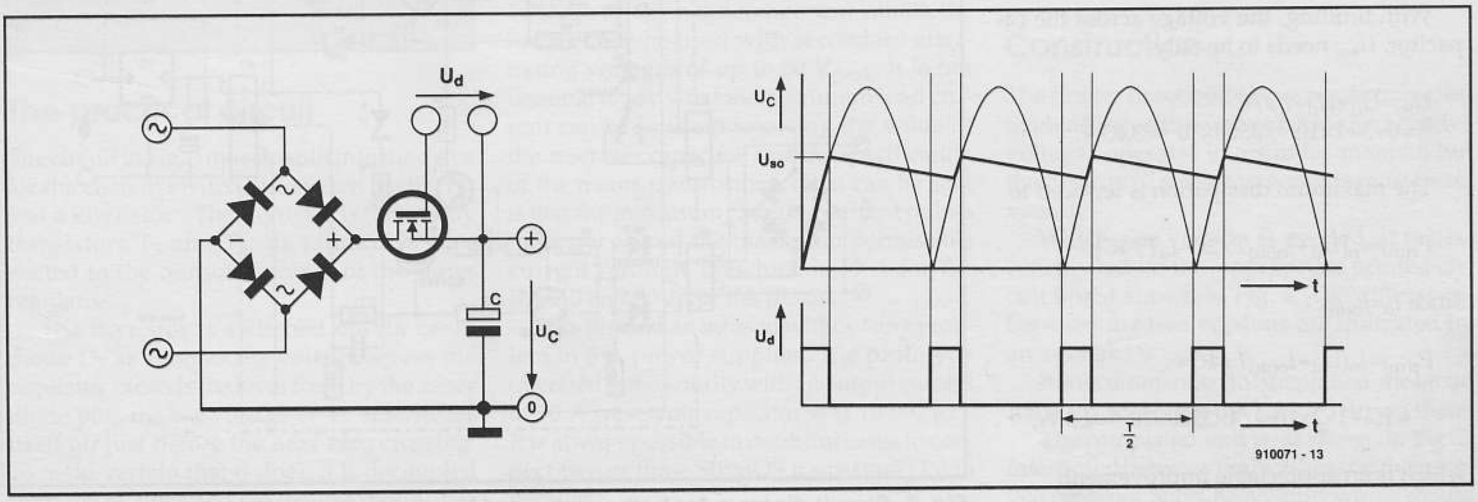


Fig. 1. Principle of operation of the dissipation limiter.

and the potential, U_c, across the capacitor follows the instantaneous level of the half-wave voltage. When U_c has reached the minimum level, U_{so}, required for the wanted output voltage, U_o, the charging current is switched off until the end of the half cycle. The level of U_{so} must be chosen to ensure that U_c does not drop below U_r until charging current begins to flow again at the start of the next half cycle. This voltage is the sum of the wanted output voltage, the drop across the regulator, U_d, and the voltage resulting from the discharging of the capacitor. The difference ΔU that is, the series switch-off voltage, $U_{so(m)}$, between U_r and U_{so} is easily determined, since it is directly proportional to the charging current; in fact, $\Delta U = It/C$, where I is the charging current, t is the time during which charging current flows, and C is the capacitance of the reservoir capacitor. Thus,

$$U_{so} = U_o + U_d + \Delta U$$

$$= U_o + U_d + It/C.$$

The time t is, in full-wave rectification, equal to a half cycle of the mains frequency, that is, $T/2$. Then,

$$U_{so} = U_o + U_d + IT/2C.$$

If now the maximum permissible output current, $I_{o(m)}$ is substituted for I, the highest potential drop across the regulator (at the start of each half cycle) is

$$U_{so(m)} = U_{so} - U_o = U_d + I_{o(m)}T/2C.$$

From this, the instantaneous dissipation, P_r, can be computed:

$$P_r = I_o U_{so(m)} = I_o[U_d + I_{o(m)}T/2C - I_o T/4C].$$

As an example: a power supply with a reservoir capacitor of 3 300 µF is required to provide an output voltage of 0–15 V at a maximum current of 1 A. Since the potential drop across the regulator is 3 V, the voltage across the capacitor, U_c, must be at least 18 V. Without limiting, the maximum power loss, $P_{r(m)}$, in the regulator is 18×1=18 W (which is, for instance, the case when maximum current flows at very low output voltage as in a short-circuit condition).

With limiting, the voltage across the capacitor, U_{so}, needs to be only

$$U_{so} = U_o + U_d + I_o t/C =$$
$$= 0 + 3 + 1\times10^{-2}/3300\times10^{-6} = 3.03 \text{ V}.$$

The maximum dissipation is reduced to

$$P_{r(m)} = I_o[U_d + I_{o(m)}T/2C - I_o T/4C].$$

Since $I_o = I_{o(m)}$,

$$P_{r(m)} = I_o(U_d + I_{o(m)}T/4C =$$

$$= 1(3 + 1\times2\times10^{-2}/4\times3300\times10^{-6} = 4.5 \text{ W},$$

which is an appreciable improvement.

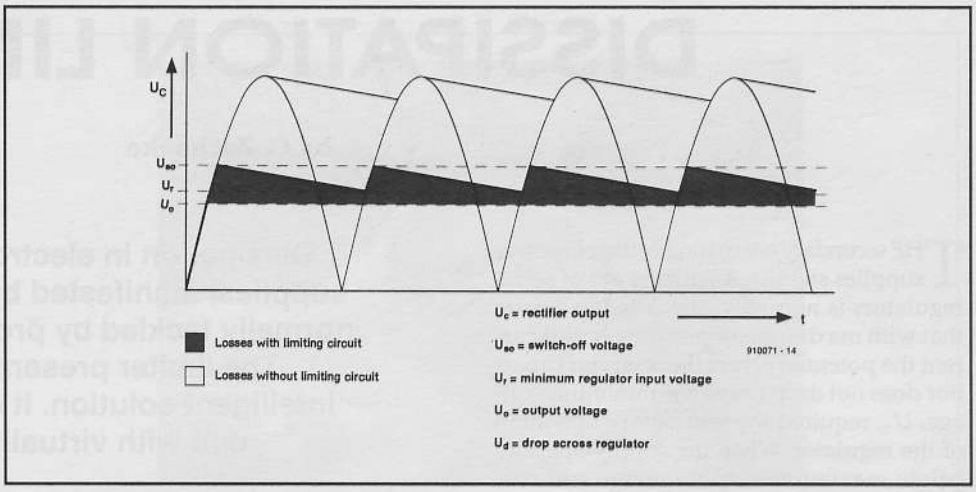


Fig. 2. Dissipation with and without limiter.

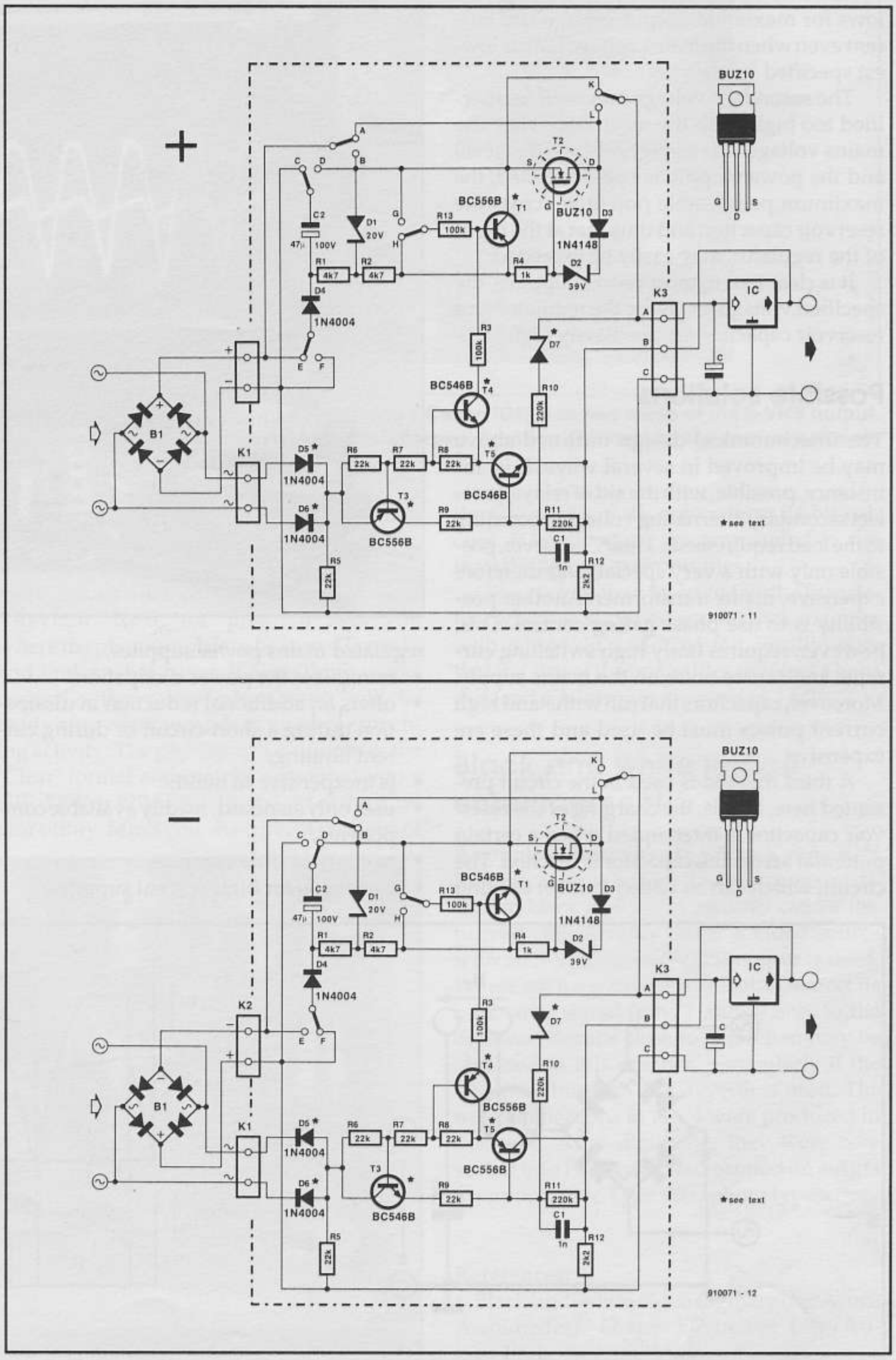


Fig. 3. Circuit diagram for both versions of the dissipation limiter.

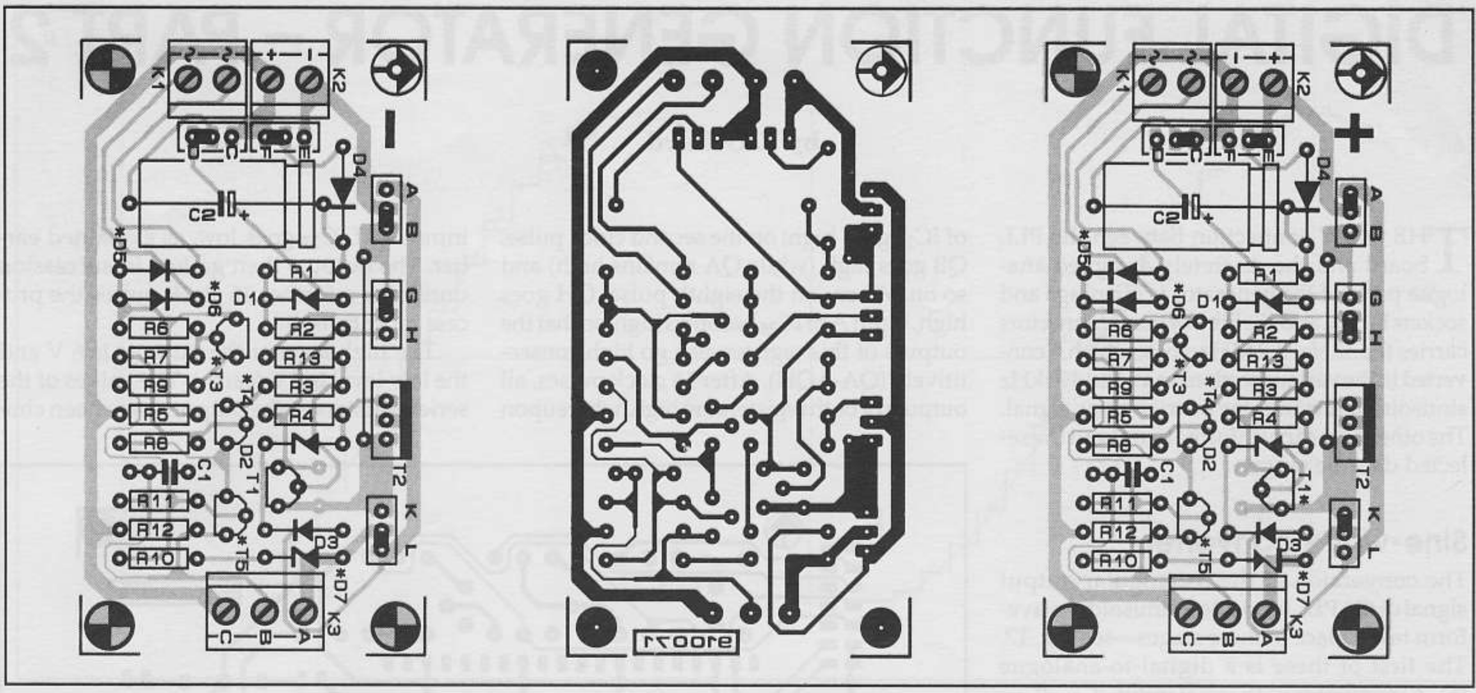


Fig. 4. Printed circuit boards are available for both versions of the dissipation limiter.

PARTS LIST

Resistors:
R1, R2 = 4.7 kΩ
R3 = 100 kΩ
R4 = 1 kΩ
R5–9 = 22 kΩ
R10, R11 = 220 kΩ
R12 = 2.2 kΩ
R13 = 100 kΩ

Capacitors:
C1 = 1 nF
C2 = 47 μF, 100 V

Semiconductors:
D1 = zener diode, 20 V, 400 mW
D2 = zener diode, 39 V, 400 mW
D3 = 1N4148
D4–6 = 1N4004
D7 = see text
T1, T3 = BC556B (pos); BC546B (neg)
T2 = BUZ10 or BUZ11 (see text)
T4, T5 = BC546B (pos); BC556B (neg)

Miscellaneous:
Heat sink for T2
PCB 910071

The practical circuit

The circuit in Fig. 3 may be split into the drive for the current switch, the switch itself (T_2) and a 'thyristor'. The thyristor is formed by transistors T_3 and T_5; its cathode is connected to the output terminal of the series regulator.

The thyristor is switched on via zener diode D_7 as soon as the voltage across the regulator exceeds the level fixed by the zener diode plus the b-e voltage of T_5. It switches itself off just before the next zero crossing. To make certain that it does, it is decoupled from the rectifier and the inverse diode of T_2 via D_4 and D_5, which are loaded by R_5.

When the thyristor is on, T_4 switches T_1 on and this in turn switches T_2 off.

Transistor T_4 also serves, in conjunction with R_3, to decouple the thyristor and the charging-current switch.

Diode D_4 and C_2 provide T_2 with the necessary switching voltage.

Zener diode D_1 protects the gate of T_2 against overvoltage.

The inductance of the mains transformer causes a high back e.m.f. when the charging current is switched off, and this may upset the correct operation of T_2. This is prevented by D_2 and D_3, which switch off T_2 as soon as the back e.m.f. exceeds the permissible reverse bias. A useful effect of the back e.m.f. is that it increases the potential across C_2, which guarantees satisfactory switching of T_2 even when the output voltage is a maximum.

Resistor R_{12} ensures correct switching of T_2 when the output is not loaded (open circuit). It must be rated at $U_{o(m)}{}^2/R_{12}$ Watt. It may be omitted if the power supply is permanently loaded.

Transistor T_2 must be fitted, *insulated*, on its own heat sink or on that of the regulator.

Depending on the component values, the limiter may be used with secondary alternating voltages of up to 50 V_{peak}. It is not possible to say what the maximum load current can be without knowing the value of the reservoir capacitor and the specification of the mains transformer. What can be said is that the maximum charging current pulses must not exceed the maximum permissible current through T_2, which is 19 A for the BUZ10 and 30 A for the BUZ11.

The limiter can be used without any problem in 5 A power supplies. The prototype operated satisfactorily with an output current of 10 A (reservoir capacitor was 10 000 μF). It is always possible in doubtful cases to connect two or three SIPMOS transistors (T_2) in parallel.

Here are some tips for calculating the values or ratings of a number of components.

- The zener voltage of D_7 must be U_{so}–0.7 V ($U_{b\text{-}e}$ of T_5).
- The maximum reverse bias of T_2 must be greater than the peak value of the potential across the reservoir capacitor.
- The zener voltage of D_2 must be equal to the maximum reverse bias of T_2 minus 5 V.
- Capacitor C_2 must be rated at $U_{so(m)}$ plus 20 V (D_1).
- Transistor T_4 must be able to withstand voltages of $U_{so(m)}$ plus 20 V (D_1).
- Transistors T_3 and T_5 must have a reverse bias rating equal to the peak value of the secondary alternating voltage.
- Resistor R_{12} must be rated at $U_{o(m)}{}^2/R_{12}$ (watts).
- All connecting wires should be as short as possible and of appropriate thickness.
- The dimensions of the heat sink depend on the transformer, the reservoir capacitor and the maximum permissible short-circuit current.
- In most cases, it is possible to fit T_2 on the heat sink of the regulator.

Construction

The limiter described above is, of course, intended for positive voltages. One for negative voltages operates in a similar manner, but the polarity of some components must be reversed.

Whichever version is needed, it is best constructed on the appropriate printed-circuit board shown in Fig. 4. The differences between the two versions are indicated by an asterisk (*).

It is recommended to 'strengthen' the broad tracks by soldering thick, bare wire on them.

The completed unit is, as shown in Fig. 3, interposed between the rectifier and the reservoir capacitor. Short, heavy-duty wiring should be used. ■